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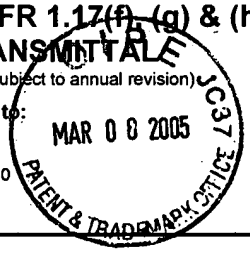

Application Number	10/787,269
Filing Date	February 25, 2004
First Named Inventor	Chien-Ping Huang
Art Unit	2814
Examiner Name	W. M. Fahmy
Attorney Docket Number	58102-DIV (71987)

Enclosed is a petition filed under 37 CFR 1.102(d) **that requires a processing fee (37 CFR 1.17(f)), (g), or (h)). Payment of $** 130.00 **is enclosed.**

This form should be included with the above-mentioned petition and faxed or mailed to the Office using the appropriate Mail Stop (e.g., Mail Stop Petition), if applicable. *For transmittal of processing fees under 37 CFR 1.17(i), see form PTO/SB/17i.*

Payment of Fees (small entity amounts are NOT available for the petition fees).

[X] The Commissioner is hereby authorized to charge the following fees to Deposit Account No. 04-1105 :
[X] Petition fee under 37 CFR 1.17(f), (g) or (h) [X] Any deficiency of fees and credit of any overpayments
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Petition Fees under 37 CFR 1.17(f): Fee $400 Fee Code 1462

For petitions filed under:
§ 1.53(e) – to accord a filing date.
§ 1.57(a) – to accord a filing date.
§ 1.182 – for decision on a question not specifically provided for.
§ 1.183 – to suspend the rules.
§ 1.378(e) – for reconsideration of decision on petition refusing to accept delayed payment of maintenance fee in an expired patent.
§ 1.741(b) – to accord a filing date to an application under § 1.740 for extension of a patent term.

Petition Fees under 37 CFR 1.17(g): Fee $200 Fee Code 1463

For petitions filed under:
§ 1.12 – for access to an assignment record.
§ 1.14 – for access to an application.
§ 1.47 – for filing by other than all the inventors or a person not the inventor.
§ 1.59 – for expungement of information.
§ 1.103(a) – to suspend action in an application.
§ 1.136(b) – for review of a request for extension of time when the provisions of section 1.136(a) are not available.
§ 1.295 – for review of refusal to publish a statutory invention registration.
§ 1.296 – to withdraw a request for publication of a statutory invention registration filed on or after the date the notice of intent to publish issued.
§ 1.377 – for review of decision refusing to accept and record payment of a maintenance fee filed prior to expiration of a patent.
§ 1.550(c) – for patent owner requests for extension of time in ex parte reexamination proceedings.
§ 1.956 – for patent owner requests for extension of time in inter partes reexamination proceedings.
§ 5.12 – for expedited handling of a foreign filing license.
§ 5.15 – for changing the scope of a license.
§ 5.25 – for retroactive license.

Petition Fees under 37 CFR 1.17(h): Fee $130 Fee Code 1464

For petitions filed under:
§ 1.19(g) – to request documents in a form other than that provided in this part.
§ 1.84 – for accepting color drawings or photographs.
§ 1.91 – for entry of a model or exhibit.
§ 1.102(d) – to make an application special.
§ 1.138(c) – to expressly abandon an application to avoid publication.
§ 1.313 – to withdraw an application from issue.
§ 1.314 – to defer issuance of a patent.

Signature	March 8, 2005 Date
Steven M. Jensen Typed or printed name	42,693 Registration No., if applicable

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV517930715US, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Dated: March 8, 2005 Signature: Michelle Chicos (Michelle Chicos)

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PATENT & TRADEMARK OFFICE

Docket No. 58102-DIV (71987)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	C. Huang		
U.S. SERIAL NO.:	10/787,269	GROUP:	2814
FILED:	February 25, 2004	EXAMINER:	W. Fahmy
FOR:	SEMICONDUCTOR PACKAGE WITH HEAT DISSIPATING STRUCTURE		

CERTIFICATE OF EXPRESS MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on this date March 8, 2005 in an envelope as "Express Mail Post Office to Addressee," mailing Label Number EV517930715US addressed to the: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

By: Michelle Chicos
Michelle P. Chicos

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

PETITION TO MAKE SPECIAL – ACCELERATED EXAMINATION, PURSUANT TO 37 CFR 1.102(d) AND MPEP 708.02 VIII

Pursuant to 37 C.F.R. §1.102(d) and MPEP 708.02 VIII, Applicant respectfully petitions to have the subject application granted Special status under the accelerated examination procedure.

As required under MPEP 708.02 VIII, Applicant submits the following:

03/14/2005 JBALINAN 00000117 041105 10787269
01 FC:1464 130.00 DA

(A) A petition accompanied by the fee set forth in 37 CFR 1.17(h). Please charge our Deposit Account No. 04-1105 in the amount of $130.00 covering the fee set forth in 37 CFR 1.17(h).

(B) A Preliminary Amendment accompanies this petition. It is believed that all claims are directed to a single invention. In the event the U.S. Patent and Trademark Office determines that all the claims presented are not obviously directed to a single invention, Applicant agrees to make an election without traverse.

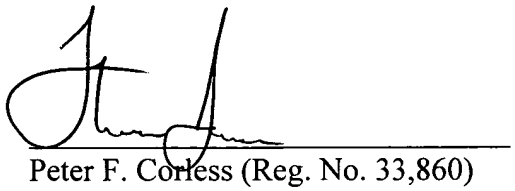
(C) A pre-examination search has been made. See the attached document titled "PRE-EXAMINATION SEARCH". An Information Disclosure Statement (IDS) was filed with the present application, including references cited by the Examiner in the parent application, U.S. Serial No. 10/211,430 (now U.S. Patent No. 6,720,649). Additional references have been cited in an IDS accompanying this petition, and discussed in the attached "PRE-EXAMINATION SEARCH" document. In the parent application, searches were made in class 257, subclasses 691, 706, 707, 718, 719, 778, 787, and 796, along with keyword searches in classes 257 and 438. Applicant's pre-examination search has updated these search areas.

(D) Several references from the pre-examination search are already of record (see IDS filed on February 25, 2004). As noted above, additional references have been cited in an IDS accompanying this petition.

(E) A detailed discussion of the references is provided in the attached "PRE-EXAMINATION SEARCH" document, including an explanation of how the claimed subject matter is patentable over the references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 04-1105, under Order No. 58102 (71987).

Respectfully submitted,



Date: March 8, 2005

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Docket No. 58102-DIV (71987)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	C. Huang		
U.S. SERIAL NO.:	10/787,269	GROUP:	2814
FILED:	February 25, 2004	EXAMINER:	W. Fahmy
FOR:	SEMICONDUCTOR PACKAGE WITH HEAT DISSIPATING STRUCTURE		

CERTIFICATE OF EXPRESS MAILING

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By: Michelle P. Chicos
Michelle P. Chicos

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

PRELIMINARY AMENDMENT

Applicant kindly requests that the above-identified application be amended as follows:

Amendments to the claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 7 of this paper.

Amendments to the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claims 1-15 (canceled)

Claim 16 (previously presented): A heat dissipating structure for a semiconductor package having a substrate, at least a chip mounted on the substrate and electrically connected to the substrate via a plurality of conductive elements, and one or more passive components mounted on the substrate, the heat dissipating structure comprising:

a flat portion; and

a plurality of support portions formed at edges of the flat portion for supporting the flat portion in position above the chip, wherein the support portions are mounted at a predetermined area on the substrate and free of interference with an arrangement of the chip, the passive components and the conductive elements, and the support portions are arranged to form a space between two adjacent support portions, the space being sufficiently dimensioned to accommodate the conductive elements and the passive components so as to allow the conductive elements to pass through the space to reach an area on the substrate outside coverage of the heat dissipating structure and such that the passive components are located within and/or outside the coverage of the heat dissipating structure.

Claim 17 (currently amended): The heat dissipating structure of claim ~~1~~16, wherein the conductive elements are bonding wires, and a plurality of bond fingers are formed on the substrate for allowing the bonding wires to be bonded to the bond fingers.

Claim 18 (currently amended): The heat dissipating structure of claim ~~2~~17, wherein the flat portion is elevated above the chip by the support portions and forms a predetermined height

difference with respect to the substrate, allowing the height difference to be larger than a height of wire loops of the bonding wires.

Claim 19 (currently amended): The heat dissipating structure of claim ~~3~~18, wherein part of the bond fingers are situated on the substrate at an area outside the coverage of the heat dissipating structure, allowing the corresponding bonding wires to pass through the space embraced by adjacent support portions and the flat portion and to reach the outside-coverage bond fingers.

Claim 20 (currently amended): The heat dissipating structure of claim ~~1~~16, wherein the support portions are situated at edge corners of the flat portion.

Claim 21 (currently amended): The heat dissipating structure of claim ~~1~~16, wherein the chip and the conductive elements are encapsulated by an encapsulant formed on the substrate.

Claim 22 (currently amended): The heat dissipating structure of claim ~~6~~21, wherein the flat portion has a top surface exposed to outside of the encapsulant, and a bottom surface opposed to the top surface, the bottom surface being formed with the support portions.

Claim 23 (currently amended): The heat dissipating structure of claim ~~7~~22, wherein at least a protrusion is formed on the bottom surface of the flat portion and extends toward the chip.

Claim 24 (currently amended): The heat dissipating structure of claim ~~7~~22, wherein at least a peripherally-situated recess is formed on the top surface of the flat portion.

Claim 25 (currently amended): The heat dissipating structure of claim ~~1~~16, wherein each of the support portions is formed with at least a hole for allowing an encapsulating resin used for forming the encapsulant to pass through the hole.

Claim 26 (currently amended): The heat dissipating structure of claim ~~1~~16, wherein each of the support portions is formed with a contact portion at a position in contact with the substrate.

Claim 27 (currently amended): The heat dissipating structure of claim ~~11~~26, wherein the contact portion substantially extends laterally with respect to the substrate.

Claim 28 (currently amended): The heat dissipating structure of claim ~~11~~26, wherein the contact portion is of a triangular, rectangular or semicircular shape.

Claim 29 (previously presented): A heat dissipating structure for a semiconductor package having a plurality of conductive elements and one or more passive components, comprising:

a flat portion having a top surface and a bottom surface opposed to the top surface; and

a plurality of support portions formed at edge corners of the bottom surface of the flat portion, wherein the support portions are arranged to form a space between two adjacent support portions, and the space is sufficiently dimensioned to accommodate the conductive elements and the passive components.

Claim 30 (currently amended): The heat dissipating structure of claim ~~14~~29, wherein the conductive elements are bonding wires, such that the space is dimensioned to have a predetermined height larger than a height of wire loops of the bonding wires.

Claim 31 (currently amended): The heat dissipating structure of claim ~~14~~29, wherein at least a protrusion is formed on the bottom surface of the flat portion.

Claim 32 (currently amended): The heat dissipating structure of claim ~~14~~29, wherein the top surface of the flat portion is exposed to outside of the semiconductor package.

Claim 33 (currently amended): The heat dissipating structure . of claim ~~17~~32, wherein at least a peripherally-situated recess is formed on the top surface of the flat portion.

Claim 34 (currently amended): The heat dissipating structure of claim ~~14~~29, wherein each of the support portions is formed with at least a hole for allowing an encapsulating resin used in the semiconductor package to pass through the hole.

Claim 35 (currently amended): The heat dissipating structure of claim ~~14~~29, wherein each of the support portions has one end attached to the flat portion and the other end formed with a contact portion.

Claim 36 (currently amended): The heat dissipating structure of claim ~~20~~35, wherein the contact portion substantially extends laterally with respect to the flat portion.

Claim 37 (currently amended): The heat dissipating structure of claim ~~20~~35, wherein the contact portion is of a triangular, rectangular or semicircular shape.

Claim 38 (previously presented): A heat dissipating structure for a semiconductor package having a plurality of bonding wires and one or more passive components, comprising:

a flat portion having a top surface and a bottom surface opposed to the top surface; and

a plurality of support portions formed at edge corners of the bottom surface of the flat portion, wherein the support portions are arranged to form a space between two adjacent support portions, and the space is dimensioned to have a predetermined height larger than a height of wire loops of the bonding wires and a height of the passive components.

Claim 39 (currently amended): The heat dissipating structure of claim ~~23~~38, wherein at least a protrusion is formed on the bottom surface of the flat portion.

Claim 40 (currently amended): The heat dissipating structure of claim ~~23~~38, wherein the top surface of the flat portion is exposed to outside of the semiconductor package.

Claim 41 (currently amended): The heat dissipating structure of claim ~~25~~40, wherein at least a peripherally-situated recess is formed on the top surface of the flat portion.

Claim 42 (currently amended): The heat dissipating structure of claim ~~23~~38, wherein each of the support portions is formed with at least a hole for allowing an encapsulating resin used in the semiconductor package to pass through the hole.

Claim 43 (currently amended): The heat dissipating structure of claim ~~23~~38, wherein each of the support portions has one end attached to the flat portion and the other end formed with a contact portion.

Claim 44 (currently amended): The heat dissipating structure of claim ~~28~~43, wherein the contact portion substantially extends laterally with respect to the flat portion.

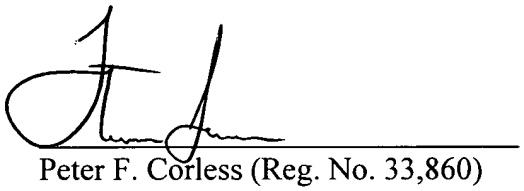
Claim 45 (currently amended): The heat dissipating structure of claim ~~28~~43, wherein the contact portion is of a triangular, rectangular or semicircular shape.

REMARKS

Claims 16-45 are pending in the application. Claims 17-28, 30-37, and 39-45 have been amended to correct claim dependencies. No new matter is presented by virtue of this amendment.

Applicant respectfully requests entry of this amendment prior to examination. Early consideration and allowance of the application are earnestly solicited.

Respectfully submitted,



Date: March 8, 2005

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PRE-EXAMINATION SEARCH

This divisional application claims a heat dissipating structure for a semiconductor package that includes a substrate, at least a chip mounted on the substrate and electrically connected to the substrate via a plurality of conductive elements such as bonding wires, and one or more passive components mounted on the substrate. The heat dissipating structure comprises a flat portion, and a plurality of support portions formed at edges (corners) of the flat portion for supporting the flat portion in position above the chip. The support portions are mounted on the substrate and do not interfere with an arrangement of the chip, the passive components and the bonding wires. Moreover, the support portions are arranged to form a space between any two adjacent support portions, wherein the space is sufficiently dimensioned to accommodate the bonding wires and the passive components, such that the bonding wires can pass through the space to reach an area on the substrate outside the area covered by the heat dissipating structure, and the passive components can be located outside the area covered by the heat dissipating structure.

By the use of such heat dissipating structure in a semiconductor package, bonding wires, passive components and/or other electrical components can be disposed on an area of the substrate outside the area covered by the heat dissipating structure, and the surface area of the substrate occupied by the heat dissipating structure is reduced. As a result, the available space on the substrate for electrical components is increased, and the components can be more flexibly arranged in the semiconductor package.

Prior Arts Relating to Heat Dissipating Structure for Semiconductor Package

1. U.S. Patent No. 5,397,917 to Ommen et al. (hereinafter "Ommen")

Ommen discloses a protective metal cap incorporated in a semiconductor

package. As shown in FIG. 1, the semiconductor package includes a heat spreader 11, a semiconductor die 25 mounted to the heat spreader 11, conductive wires 29 for electrically connecting the die 25 to conductive traces 20 formed on the heat spreader 11, and the protective metal cap 30 for covering the die 25 and conductive wires 29. In column 5, lines 7-45, the protective cap 30 covers and protects the die 25 from mechanical stresses as well as serves as a heat spreader by promoting heat removal from the die 25. The protective cap 30 comprises a coined sheet of metal that includes a central depression 36, a raised portion 35 surrounding the central depression 36, and lips 31 along the periphery of the sheet of metal to rigidize the edge. The central depression 36 is close to the die 25 for facilitating heat transfer away from the die 25. The raised portion 35 allows the protective cap 30 to be over the conductive wires 29 without touching them. The lips 31 prevent solder mask 26 or adhesive 27 from being squeezed out from under and around he edge of the protective cap 30.

In Ommen, the above specific structure of the protective cap 30 defines an enclosed space under the central depression 36 and surrounded by the raised portion 35; since there is no encapsulation resin over or around the protective cap 30, the die 25 and conductive wires 29 must be received in the enclosed space to be hermetically isolated from the atmosphere.

Ommen does not teach or suggest a heat dissipating structure including a flat portion and a plurality of support portions at corners of the flat portion, wherein a space is formed between any two adjacent support portions such that bonding wires can pass through the space to reach an area on the substrate outside the area covered by the heat dissipating structure and passive components can also be located at the outside area as claimed in the present invention. Moreover, the specific structure of the protective cap 30 and the intended purposes (except for heat dissipation) achieved thereby in Ommen are different from those of the heat dissipating structure in the present invention.

2. U.S. Patent No. 5,468,910 to Knapp et al. (hereinafter "Knapp")

Knapp discloses a protective lid mounted in a semiconductor device package.

As shown in FIG. 1, the semiconductor device package includes a semiconductor die 16 attached to a heatsink 10, wires 18 for electrically connecting the die 16 to a printed wire board 12, the protective lid 20 over the die 16 and attached to the substrate 10, and a molding compound 28 for partially encapsulating the protective lid 20. The protective lid 20 prevents the molding compound 28 from contacting the die 16 and wires 18, such that disadvantages caused by molding compound contacting the die 16 and wires 18 are avoided. A portion 30 of the protective lid 20 remains exposed from the molding compound 28 and provides superior heat dissipation for the package.

In Knapp, for preventing the molding compound 28 from contacting the die 16 and wires 18, the protective lid 20 must define an enclosed space where the die 16 and wires 18 are received and isolated from the molding compound 28.

Knapp does not teach or suggest a heat dissipating structure including a flat portion and a plurality of support portions at corners of the flat portion, wherein a space is formed between any two adjacent support portions such that bonding wires can pass through the space to reach an area on the substrate outside the area covered by the heat dissipating structure and passive components can also be located at the outside area as claimed in the present invention. Moreover, the structure of the protective lid 20 in Knapp is different from the heat dissipating structure in the present invention, and the purpose of the protective lid 20 to prevent the molding compound 28 from contacting the die 16 and wires 18 is silent in the present invention.

3. U.S. Patent No. 5,543,663 to Takubo

Takubo relates to a positional relationship between a semiconductor device e.g. a TCP (tape carrier package) and a heat sink on a printed circuit board. As shown in FIGs. 10-12, the TCP 102 is mounted on an insulating board 11, and the heat sink 103 is mounted on the insulating board 11 and covers the TCP 102. As shown in FIGs. 7-9 (column 20, lines 58-61), the TCP 102 comprises a TAB tape constituted by a polyimide tape 13 and leads 14, a semiconductor chip 15 connected to one end of each of the leads 14, and a potting resin 16 which covers

the semiconductor chip 15. The heat sink 103 comprises a lid portion 17 and fin portions 18. In one embodiment, as shown in FIGs. 13-15 and column 21, lines 21-56, the lid portion 17 comprises a square plate portion and projecting portions formed at the four corners of the plate portion. The fin portions 18 are mounted on the plate portion of the lid portion 17. The total surface area of the fin portions 18 is maximized to facilitate heat diffusion. The lid portion 17 and the fin portions 18 may be or may not be integrally formed.

The problem to be solved by Takubo is to eliminate damage to the TCP 102 caused by a conventional heat sink 103 that is directly mounted on the TCP 102 and difficult for the leads 14 to support the mass of the heat sink 103 according to FIGs. 157 and 158.

The lid portion 17 in Takubo may be slightly similar to the heat dissipating structure in the present invention in terms of the four projecting portions being provided at the corners of the lid portion 17. However, the heat sink 103 in Takubo is essentially different from the heat dissipating structure in the present invention as the heat sink 103 is not for use in a semiconductor package. The heat sink 103 in Takubo is mounted on a printed circuit board and covers a semiconductor device e.g. TCP 102. On the contrary, the heat dissipating structure in the present invention is for use in a semiconductor package and specifically structured to allow bonding wires in the semiconductor package to reach an area on the substrate outside the area covered by the heat dissipating structure; such structural arrangement is not taught or suggested in Takubo. The heat sink 103 in Takubo covers the entire TCP 102. There is no teaching or suggestion in Takubo that any element or component of the TCP 102 would pass through a space between two adjacent projecting portions of the lid portion 17 to reach an area on the printed circuit board outside the area covered by the heat sink 103. Moreover, apart from heat dissipation, the problem to be solved by Takubo to eliminate damage to the TCP 102 is completely different from that in the present invention. On the other hand, the intended effects achieved by the heat dissipating structure in the present invention cannot be attained according to Takubo since the heat sink 103 is not for use in a semiconductor package.

4. U.S. Patent No. 5,982,621 to Li

Li discloses a heat sink and a BGA (ball grid array) package with the heat sink. As shown in FIGs. 1-3, the heat sink 10 includes a mounting section 13, a supporting frame section 12, and a face panel section 11. The supporting frame section 12 supports the face panel section 11 on the mounting section 13. A downwardly tapered through hole 111 is formed at the center of the face panel section 11, and a tapered heat conductive block 20 is fastened to the tapered through hole 111. Referring to FIG. 4, when the heat sink 10 is mounted on a substrate 30 of the BGA package, a CPU 31 and wires 32 are completely received in a space defined under the face panel section 11 and surrounded by the supporting frame section 12.

Therefore, Li does not teach or suggest a heat dissipating structure including a flat portion and a plurality of support portions at corners of the flat portion, wherein a space is formed between any two adjacent support portions such that bonding wires can pass through the space to reach an area on the substrate outside the area covered by the heat dissipating structure and passive components can also be located at the outside area as claimed in the present invention.

Moreover, Li may encounter a problem that the heat sink 10 with the encircled supporting frame section 12 occupies a substantial portion of the surface area on the substrate 30 and reduces the surface area available for accommodating electronic components on the substrate 30. This problem is specifically addressed by the present invention.

5. U.S. Patent No. 6,229,702 to Tao et al. (hereinafter "Tao")

Tao discloses a heat sink mounted in a BGA semiconductor package. As shown in FIG. 1, the BGA package includes a substrate 12, a plurality of solder balls 15 formed on a lower surface of the substrate 12, a die 11 attached to an upper surface of the substrate 12 and electrically coupled to the substrate 12 by bonding wires 16; and a heat sink 10 mounted on the substrate 12 to cover the die 11. Referring to FIGs. 2A and 2B, column 3, lines 13-21, the heat sink 10 is of

rectangular shape having a protrusion area 101 in a center portion thereof. The heat sink 10 has four dents 102 formed on the four corners thereof, respectively, such that the heat sink 10 can stand on the substrate 12 by the dents 102. The protrusion area 101 covers the die 11 and bonding wires 16 to provide heat dissipation effect.

Such heat sink 10 in Tao may be slightly similar to the heat dissipating structure in the present invention in terms of the four corner dents 102 being provided and attached to the substrate 12. However, Tao explicitly indicates that the protrusion area 101 covers the die 11 and bonding wires 16, such that the bonding wires 16 would not pass though a space between two adjacent dents 102 of the heat sink 10. And Tao does not teach or suggest that a space between two adjacent dents 102 is sufficiently dimensioned to accommodate bonding wires 16. Therefore, the heat sink 10 in Tao is different from the heat dissipating structure in the present invention.

6. U.S. Patent No. 6,359,341 to Huang et al. (hereinafter "Huang (I)")

Huang (I) discloses a heat spreader 7 incorporated in a BGA semiconductor package as shown in FIG. 3. In column 6, lines 42-56, the heat spreader 7 has a flat portion 70 and a skirt portion 71. The skirt portion 71 can be bonded to a ground metallic layer 32. The chip and wires are completely received in a space defined under the flat portion 70 and surrounded by the skirt portion 71.

Therefore, Huang (I) does not teach or suggest a heat dissipating structure including a flat portion and a plurality of support portions at corners of the flat portion, wherein a space is formed between any two adjacent support portions such that bonding wires can pass through the space to reach an area on the substrate outside the area covered by the heat dissipating structure and passive components can also be located at the outside area as claimed in the present invention.

7. U.S. Patent No. 6,462,405 to Lai et al. (hereinafter "Lai")

Lai discloses a semiconductor package, as shown in FIG. 1, which is

characterized by attaching a lid 33 to a semiconductor chip 31. The lid 33 is made from a defective die having the same coefficient of thermal expansion as that of the chip 31. And the lid 33 provides the chip 31 with a better mechanical strength so as to reduce a thermal stress effect on the chip 31 and prevent cracks of the chip 31. The semiconductor package also comprises a heat sink 34. In column 4, line 58-61, the heat sink 34 is constructed by a plane 340 and support members 341 for positioning the plane 340 above the semiconductor chip 31 without contacting the lid 33 and gold wires 32.

From FIG. 1 of Lai, it shows that the chip 31 and gold wires 32 are completely received in a space defined by the plane 340 and support members 341. Lai does not teach or suggest any gold wires 32 to pass through a space between two adjacent support members 341 to reach an area on the substrate 30 outside the area covered by the heat sink 34. The heat sink 34 is not a characteristic feature of Lai to achieve the intended improvement, but the lid 33 is. Thus the specific structural arrangement of the heat dissipating structure in the present invention and the problem to be solved thereby are not taught or suggested in Lai.

8. U.S. Patent No. 6,552,428 to Huang et al. (hereinafter "Huang (II)")

Huang (II) discloses an exposed heat spreader mounted in a semiconductor package. As shown in FIGs. 1-3, column 5, lines 29-51, the heat spreader 4 includes a lower portion 40, an upper portion 41, and connecting parts 42. Two supporting parts 403 are provided to make the lower portion 40 keep a predetermined distance from the substrate 2. The connecting parts 42 connect the lower portion 40 and the upper portion 41 to form a containing space 43 for containing the chip 3 and making the chip 3 and gold wires 6 untouched with the heat spreader 4.

The heat spreader 4 in Huang (II) is different from the heat dissipating structure in the present invention. In other words, Huang (II) does not teach or suggest a heat dissipating structure including a flat portion and a plurality of support portions at corners of the flat portion, wherein a space is formed between

any two adjacent support portions and sized sufficiently such that bonding wires can pass through the space to reach an area on the substrate outside the area covered by the heat dissipating structure and passive components can also be located at the outside area as claimed in the present invention.

U.S. Patent No. 5,977,626 to Wang et al.

Wang et al. (hereinafter "Wang") is cited in the specification and was also cited by the examiner in the parent application.

As discussed in the Background section with reference to FIGs. 5 and 6, Wang teaches a heat dissipating structure 33 comprising a flat portion 330 and a single encircled support portion 331. The flat portion 330 and the single encircled support portion 331 integrally defines an enclosed receiving space 35 for receiving the chip 31, bonding wires 32 and passive components therein. The encircled support portion occupies a substantial portion of the surface area on the substrate, thereby reducing the surface area available for accommodating electronic components on the substrate.

The present invention specifically addresses the above deficiency and proposes the invented heat dissipating structure including a flat portion and a plurality of support portions at corners of the flat portion, wherein a space is formed between any two adjacent support portions and sized sufficiently such that bonding wires can pass through the space to reach an area on the substrate outside the area covered by the heat dissipating structure and passive components can also be located at the outside area. By such heat dissipating structure in the present invention, flexibility in component arrangement and layout area on the substrate for accommodating electronic components can be increased for a semiconductor package with the heat dissipating structure.

Other Prior Arts Cited by the Examiner in the Parent Application

1. U.S. Patent No. 5,652,461 to Ootsuki et al. (hereinafter "Ootsuki")

Ootsuki discloses a convex heat sink incorporated in a lead-frame-based

semiconductor device. As shown in FIG. 1A, the heat sink 4a is mounted on a side of leads 1 of the lead frame, and a semiconductor chip 3 is attached to the heat sink 4a and electrically connected to an opposite side of the leads 1 through wires 5.

In Ootsuki, the heat sink 4a having a convex shape can improve the adhesive property of sealing resin to the heat sink 4a and keep stable quality of wire bonding. The heat sink 4a does not directly relate to the distribution of wires 5 located on the opposite side of the leads 1. Therefore, Ootsuki does not teach or suggest a heat dissipating structure including a flat portion and a plurality of support portions at corners of the flat portion, wherein a space is formed between any two adjacent support portions and sized sufficiently such that bonding wires can pass through the space to reach an area on the substrate outside the area covered by the heat dissipating structure and passive components can also be located at the outside area as claimed in the present invention.

2. U.S. Patent No. 6,246,115 to Tang et al. (hereinafter "Tang")

Tang discloses an exposed heat sink mounted in a semiconductor package. As shown in FIGs. 1-3, column 4 line 60 to column 5 line 20, the heat sink 32 is formed with a plurality of supportive legs 321 downwardly outwardly extending from the side 324 of the heat sink 32. The supportive legs 321 are used to support the heat sink. Each of the supportive legs 321 has its bottom 321c being located outside the plane of the heat sink 32, such that the substrate 30 can provide a larger chip mounting area for accommodating more chips in the package. The chips 31 and gold wires 34 are completely received in a space defined by the heat sink 32.

Tang does not teach or suggest any gold wires 34 to pass through a space between two adjacent supportive legs 321 to reach an area on the substrate 30 outside the area covered by the heat sink 32. In other words, there is not teaching or suggestion in Tang of a heat dissipating structure including a flat portion and a plurality of support portions at corners of the flat portion, wherein a space is formed between any two adjacent support portions and sized sufficiently such

that bonding wires can pass through the space to reach an area on the substrate outside the area covered by the heat dissipating structure and passive components can also be located at the outside area as claimed in the present invention.

In conclusion, the present invention is neither disclosed in any of the above references nor taught or suggested by any combination of the references.

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Dated: March 8, 2005 Signature: Michelle Chicos
(Michelle Chicos)

Docket No.: 58102-DIV (71987)
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Chien-Ping Huang

Application No.: 10/787,269 Confirmation No.: 5161

Filed: February 25, 2004 Art Unit: 2814

For: SEMICONDUCTOR PACKAGE WITH HEAT DISSIPATING STRUCTURE Examiner: W. M. Fahmy

INFORMATION DISCLOSURE STATEMENT (IDS)

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed before the mailing date of a first Office Action on the merits as far as is known to the undersigned (37 CFR 1.97(b)(3)).

Copies of the references on the PTO/SB/08 are not provided.

In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure statement shall not be construed to be an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 04-1105, under Order No. 58102-DIV (71987). A duplicate copy of this paper is enclosed.

Dated: March 8, 2005

Respectfully submitted,

By _____

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PTO/SB/08a/b (08-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/787,269-Conf. #5161
Filing Date	February 25, 2004
First Named Inventor	Chien-Ping Huang
Art Unit	2814
Examiner Name	W. M. Fahmy
Attorney Docket Number	58102DIV(71987)

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA	US-6,359,341-B1	03-19-2002	Huang et al.	
	AB	US-6,229,702-B1	05-08-2001	Tao et al.	
	AC	US-5,543,663	08-06-1996	Takubo	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

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[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature		Date Considered	

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Application No. (if known): 10/787,269 Attorney Docket No.: 58102-DIV (71987)

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IDS (Citation) by Applicant (3 References) (1 page)
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